WHAT IS CLAIMED IS:

1. A semiconductor storage device comprising:

a memory cell array in which a plurality of memory cells are arranged in an array structure, a plurality of redundant memory cells are arranged in an array structure at prescribed positions in a row direction and/or line direction of the plurality of memory cells in the array structure, a plurality of bit line pairs each composed of two bit lines arranged in almost parallel to the line direction and having wire position switching parts of the two bit lines by twisting the two bit lines at one or plural positions in the line direction is arranged, a plurality of word lines is arranged in almost parallel to the row direction, and the memory cells or the redundant memory cells are connected to the bit lines and the word lines at a plurality of crossing positions of the plurality of bit lines and the plurality of word lines;

shift-redundancy means for reassigning line addresses assigned to the plurality of bit line pairs connected to the plurality of memory cells to a plurality of other bit line pairs by sequentially shifting the line addresses in the row direction in a unit of a prescribed line address manageable number, in order to make the redundant memory cells of prescribed lines usable for data storage and reproduction instead of the plurality of memory cells of

the prescribed lines equal to the line address manageable number, and/or for reassigning row addresses assigned to the plurality of word lines connected to the plurality of memory cells to a plurality of other word lines by sequentially shifting the row addresses in the line direction in a unit of a prescribed row address manageable number, in order to make the plurality of redundant memory cells of a plurality of rows usable for the data storage and reproduction instead of the plurality of memory cells of the prescribed rows equal to the row address manageable number;

identification means for identifying the bit line pairs of which the wire position switching parts cross a word line specified by an input row address, based on twisting positions of the bit line pairs and shift of the row addresses;

determination means for determining based on an identification result of the identification means whether to invert a level of the evaluation test data to be given to the bit line pairs of which the wire position switching parts cross the word line and output from the bit line pairs; and

inversion means for, depending on a determination result of the determination means, inverting the level of the evaluation test data to be supplied to the bit line

pairs of which the wire position switching parts cross the word line at a time of storing the evaluation test data, and inverting the level of the evaluation test data output from the bit line pairs of which the wire position switching parts cross the word line at the time of reproducing the evaluation test data.

2. The semiconductor storage device according to claims 1, wherein:

the identification means identifies the bit line pairs of which the wire position switching parts cross the word line specified by the input row address, based on the twisting positions of the bit line pairs and the shift of the row addresses, at a time of storing and reproducing data other than the evaluation test data; and

the inversion means inverts, according to the determination result of the determination means, the level of the other data to be given to the bit line pairs of which the wire position switching parts cross the word line at a time of storing the other data, and the level of the other data output from the bit line pairs of which the wire position switching parts cross the word line at the time of reproducing the other data.

3. A storing and reproduction method of a semiconductor

storage device, comprising:

in a memory cell array in which a plurality of memory cells are arranged in an array structure, a plurality of redundant memory cells are arranged in an array structure at prescribed positions in a row direction and/or line direction of the plurality of memory cells in the array structure, a plurality of bit line pairs each composed of two bit lines arranged in almost parallel to the line direction and having wire position switching parts of the two bit lines by twisting the two bit lines at one or plural positions in the line direction is arranged, a plurality of word lines is arranged in almost parallel to the row direction, and the memory cells or the redundant memory cells are connected to the bit lines and the word lines at a plurality of crossing positions of the plurality of bit lines and the plurality of word lines,

a shift-redundancy step of reassigning line addresses assigned to the plurality of bit line pairs connected to the plurality of memory cells to a plurality of other bit line pairs by sequentially shifting the line addresses in the row direction in a unit of a prescribed line address manageable number, in order to make the redundant memory cells of prescribed lines usable for data storage and reproduction instead of the plurality of memory cells of the prescribed lines equal to the line address manageable

number, and/or of reassigning row addresses assigned to the plurality of word lines connected to the plurality of memory cells to a plurality of other word lines by sequentially shifting the row addresses in the line direction in a unit of a prescribed row address manageable number, in order to make the plurality of redundant memory cells of a plurality of rows usable for the data storage and reproduction instead of the plurality of memory cells of the prescribed rows equal to the row address manageable number;

an identification step for storage of, at a time of storing evaluation test data, identifying the bit line pairs of which the wire position switching parts cross a word line specified by an input row address, based on twisting positions of the bit line pairs and shift of the row addresses;

a determination step for storage of determining whether to invert a level of the evaluation test data to be given to the bit line pairs of which the wire position switching parts cross the word line, based on an identification result of the identification step for storage;

an input inversion storing step of inverting the level of the evaluation test data depending on the determination result of the determination step for storage,

and storing the evaluation test data of which the level has been inverted, in the memory cells or the redundant memory cells connected to the bit line pairs by giving the evaluation test data to the bit line pairs of which the wire position switching parts cross the word line;

an identification step for reproduction of, at a time of reproducing the evaluation test data, identifying the bit line pairs of which the wire position switching parts cross the word line specified by the input row address, based on the twisting positions of the bit line pairs and the shift of the row addresses;

a determination step for reproduction of determining whether to invert the level of the evaluation test data output from the bit line pairs of which the wire position switching parts cross the word line, based on an identification result of the identification step for reproduction; and

an output inversion reproduction step of inverting the level of the evaluation test data reproduced from the memory cells or the redundant memory cells through the bit line pairs of which the wire position switching parts cross the word line, depending on a determination result of the determination step for reproduction and outputting the evaluation test data.